WHAT IS CLAIMED IS:

1. A substrate bias generator of a semiconductor memory device having a voltage pump circuit to boost a substrate voltage in response to an input of an oscillating signal generated in an oscillator, said substrate bias generator comprising:

a substrate voltage level detector for inputting said substrate voltage and outputting a signal which drives said oscillator in response to said input level; and

a controller for inputting a chip active enable signal, a self refresh mode enable signal and an output signal of said substrate voltage level detector and for controlling a switching operation of said substrate voltage level detector in response to said input level.

2. A substrate bias generator as claimed in claim 1, wherein said substrate voltage level detector comprises:

a first PMOS transistor whose source terminal is coupled to a power supply terminal and whose gate terminal is coupled to an output signal of said controller;

first resistance means formed between said first PMOS transistor and a predetermined connecting node;

a second PMOS transistor whose source terminal is coupled to said connecting node and whose gate terminal is coupled to said substrate voltage;

second resistance means formed between said second PMOS transistor and a ground voltage terminal; and

an inverter having an input terminal coupled to said connecting node and outputting an output signal of said substrate voltage level detector.

3. A substrate bias generator as claimed in claim 2, wherein said controller comprises:

a NOR circuit inputting a reverse signal of said chip active enable signal and said self refresh enable signal, respectively; and

an AND circuit each inputting said output signal of said substrate voltage level detector and said output signal of said NOR circuit and then controlling said first PMOS transistor.

4. A substrate bias generator of a semiconductor memory device which performs refresh operations of memory cells according to said self refresh mode for refreshing said memory cells, by means of a voltage pump circuit to supply a negative voltage to a substrate, an oscillator to drive said voltage pump circuit, and a substrate voltage level detector to detect a level of said negative voltage and to drive said oscillator in response to said detecting level, said substrate bias generator comprising:

a first logic circuit inputting said chip active enable signal and said self refresh mode enable signal, respectively;

a second logic circuit inputting an output signal of said first logic circuit and an output signal of said substrate voltage level detector, respectively;

a PMOS transistor whose gate terminal is coupled to an output signal of said second logic circuit and whose source terminal is coupled to a power supply terminal, and thereby providing power supply to said substrate voltage level detector in response to said output signal of said second logic circuit.

5. A substrate bias generator as claimed in claim 4, wherein said first logic circuit is comprised of a NOR circuit.

6. A substrate bias generator as claimed in claim 4, wherein said second logic circuit is comprised of an AND circuit.